

UCD30xx General Purpose Input Output (GPIO)

Programmer's Manual

Literature Number: xxxxxx

Date

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UCD30xx general purpose input or output (GPIO) shares the same pin with other functionalities. This document explains how to configure each pin as GPIO, how to set each pin as input/output, how to read the input value if it is configured as input pin, and how to set the output value if it is configured as output pin.

GPIO_00

Register: DPWMCTRL1 – Loop 1 DPWM Control Register 1

Address FFF7ED00

Bit 16: GPIO_A_ENA – Enables GPIO mode

0 = in DPWM mode (Default)

1 = in GPIO mode

Bit 22: PWM_A_OE – Sets I/O direction when configured as GPIO

0 = configured as output (Default)

1 = configured as input

Bit 17: GPIO_A_VAL – Sets output value when configured as output

0 = driven low (Default) (driven high if polarity inverted)

1 = driven high (driven low if polarity inverted)

Register: DPWMOVERFLOW – Loop 1 DPWM Overflow Register

Address FFF7ED30

Bit 4: GPIO_A_IN – read value when configured as input

0 = observed at logic level low

1 = observed at logic level high

Register: DPWMCTRL2 – Loop 1 DPWM Control Register 2

Address FFF7ED04

Bit 6: PWM_A_INV – Sets Output Polarity

0 = Non-inverted output (Default)

1 = Inverted output

A C code example of setting this pin as digital output and driven high is shown below:

```
Dpwm1Regs.DPWMCTRL1.bit.PWM_A_OE = 0;  
Dpwm1Regs.DPWMCTRL1.bit.GPIO_A_VAL = 1;  
Dpwm1Regs.DPWMCTRL1.bit.GPIO_A_ENA = 1;
```

GPIO_01

Register: DPWMCTRL1 – Loop 1 DPWM Control Register 1

Address FFF7ED00

Bit 18: GPIO_B_ENA – Enables GPIO mode

0 = in DPWM mode (Default)

1 = in GPIO mode

Bit 23: PWM_B_OE – Sets I/O direction when configured as GPIO

0 = configured as output (Default)

1 = configured as input

Bit 19: GPIO_B_VAL – Sets output value when configured as output

0 = driven low (Default) (driven high if polarity inverted)

1 = driven high (driven low if polarity inverted)

Register: DPWMOVERFLOW – Loop 1 DPWM Overflow Register

Address FFF7ED30

Bit 5: GPIO_B_IN – read value when configured as input

0 = observed at logic level low

1 = observed at logic level high

Register: DPWMCTRL2 – Loop 1 DPWM Control Register 2

Address FFF7ED04

Bit 7: PWM_B_INV – Sets Output Polarity

0 = Non-inverted output (Default)

1 = Inverted output

GPIO_02

Register: DPWMCTRL1 – Loop 2 DPWM Control Register 1

Address FFF7E900

Bit 16: GPIO_A_ENA – Enables GPIO mode

0 = in DPWM mode (Default)

1 = in GPIO mode

Bit 22: PWM_A_OE – Sets I/O direction when configured as GPIO

0 = configured as output (Default)

1 = configured as input

Bit 17: GPIO_A_VAL – Sets output value when configured as output

0 = driven low (Default) (driven high if polarity inverted)

1 = driven high (driven low if polarity inverted)

Register: DPWMOVERFLOW – Loop 2 DPWM Overflow Register

Address FFF7E930

Bit 4: GPIO_A_IN – read value when configured as input

0 = observed at logic level low

1 = observed at logic level high

Register: DPWMCTRL2 – Loop 2 DPWM Control Register 2

Address FFF7E904

Bit 6: PWM_A_INV – Sets Output Polarity

0 = Non-inverted output (Default)

1 = Inverted output

GPIO_03

Register: DPWMCTRL1 – Loop 2 DPWM Control Register 1

Address FFF7E900

Bit 18: GPIO_B_ENA – Enables GPIO mode

0 = in DPWM mode (Default)

1 = in GPIO mode

Bit 23: PWM_B_OE – Sets I/O direction when configured as GPIO

0 = configured as output (Default)

1 = configured as input

Bit 19: GPIO_B_VAL – Sets output value when configured as output
0 = driven low (Default) (driven high if polarity inverted)
1 = driven high (driven low if polarity inverted)

Register: DPWMOVERFLOW – Loop 2 DPWM Overflow Register

Address FFF7E930

Bit 5: GPIO_B_IN – read value when configured as input
0 = observed at logic level low
1 = observed at logic level high

Register: DPWMCTRL2 – Loop 2 DPWM Control Register 2

Address FFF7E904

Bit 7: PWM_B_INV – Sets Output Polarity
0 = Non-inverted output (Default)
1 = Inverted output

GPIO_04

Register: DPWMCTRL1 – Loop 3 DPWM Control Register 1

Address FFF7E500

Bit 16: GPIO_A_ENA – Enables GPIO mode
0 = in DPWM mode (Default)
1 = in GPIO mode

Bit 22: PWM_A_OE – Sets I/O direction when configured as GPIO
0 = configured as output (Default)
1 = configured as input

Bit 17: GPIO_A_VAL – Sets output value when configured as output
0 = driven low (Default) (driven high if polarity inverted)
1 = driven high (driven low if polarity inverted)

Register: DPWMOVERFLOW – Loop 3 DPWM Overflow Register

Address FFF7E530

Bit 4: GPIO_A_IN – read value when configured as input
0 = observed at logic level low
1 = observed at logic level high

Register: DPWMCTRL2 – Loop 3 DPWM Control Register 2

Address FFF7E504

Bit 6: PWM_A_INV – Sets Output Polarity
0 = Non-inverted output (Default)
1 = Inverted output

GPIO_05

Register: DPWMCTRL1 – Loop 3 DPWM Control Register 1

Address FFF7E500

Bit 18: GPIO_B_ENA – Enables GPIO mode
0 = in DPWM mode (Default)
1 = in GPIO mode

Bit 23: PWM_B_OE – Sets I/O direction when configured as GPIO

0 = configured as output (Default)

1 = configured as input

Bit 19: GPIO_B_VAL – Sets output value when configured as output

0 = driven low (Default) (driven high if polarity inverted)

1 = driven high (driven low if polarity inverted)

Register: DPWMOVERFLOW – Loop 3 DPWM Overflow Register

Address FFF7E530

Bit 5: GPIO_B_IN – read value when configured as input

0 = observed at logic level low

1 = observed at logic level high

Register: DPWMCTRL2 – Loop 3 DPWM Control Register 2

Address FFF7E504

Bit 7: PWM_B_INV – Sets Output Polarity

0 = Non-inverted output (Default)

1 = Inverted output

GPIO_06

Register: DPWMCTRL1 – Loop 4 DPWM Control Register 1

Address FFF7E100

Bit 16: GPIO_A_ENA – Enables GPIO mode

0 = in DPWM mode (Default)

1 = in GPIO mode

Bit 22: PWM_A_OE – Sets I/O direction when configured as GPIO

0 = configured as output (Default)

1 = configured as input

Bit 17: GPIO_A_VAL – Sets output value when configured as output

0 = driven low (Default) (driven high if polarity inverted)

1 = driven high (driven low if polarity inverted)

Register: DPWMOVERFLOW – Loop 4 DPWM Overflow Register

Address FFF7E130

Bit 4: GPIO_A_IN – read value when configured as input

0 = observed at logic level low

1 = observed at logic level high

Register: DPWMCTRL2 – Loop 4 DPWM Control Register 2

Address FFF7E104

Bit 6: PWM_A_INV – Sets Output Polarity

0 = Non-inverted output (Default)

1 = Inverted output

GPIO_07

Register: DPWMCTRL1 – Loop 4 DPWM Control Register 1

Address FFF7E100

Bit 18: GPIO_B_ENA – Enables GPIO mode

0 = in DPWM mode (Default)

1 = in GPIO mode

Bit 23: PWM_B_OE – Sets I/O direction when configured as GPIO

0 = configured as output (Default)

1 = configured as input

Bit 19: GPIO_B_VAL – Sets output value when configured as output

0 = driven low (Default) (driven high if polarity inverted)

1 = driven high (driven low if polarity inverted)

Register: DPWMOVERFLOW – Loop 4 DPWM Overflow Register

Address FFF7E130

Bit 5: GPIO_B_IN – read value when configured as input

0 = observed at logic level low

1 = observed at logic level high

Register: DPWMCTRL2 – Loop 4 DPWM Control Register 2

Address FFF7E104

Bit 7: PWM_B_INV – Sets Output Polarity

0 = Non-inverted output (Default)

1 = Inverted output

GPIO_08:

Register: FAULTDIR – Fault I/O Direction Register

Address FFF7FA00

Bit 0: DIR0 – Sets I/O direction

0 = configured as input pin (Default)

1 = configured as output pin

Register: FAULTOUT – Fault Out Register

Address FFF7FA08

Bit 0: OUT0 – Sets output value when configured as output

0 = driven low (Default)

1 = driven high

Register: FAULTIN – Fault In Register

Address FFF7FA04

Bit 0: IN0 – Reads input value when configures as input

0 = observed at logic level low

1 = observed at logic level high

GPIO_09

Register: FAULTDIR – Fault I/O Direction Register

Address FFF7FA00

Bit 1: DIR1 – Sets I/O direction

0 = configured as input pin (Default)

1 = configured as output pin

Register: FAULTOUT – Fault Out Register

Address FFF7FA08

Bit 1: OUT1 – Sets output value when configured as output

0 = driven low (Default)

1 = driven high

Register: FAULTIN – Fault In Register

Address FFF7FA04

Bit 1: IN1 – Reads input value when configures as input

0 = observed at logic level low

1 = observed at logic level high

GPIO_10

Register: FAULTDIR – Fault I/O Direction Register

Address FFF7FA00

Bit 2: DIR2 – Sets I/O direction

0 = configured as input pin (Default)

1 = configured as output pin

Register: FAULTOUT – Fault Out Register

Address FFF7FA08

Bit 2: OUT2 – Sets output value when configured as output

0 = driven low (Default)

1 = driven high

Register: FAULTIN – Fault In Register

Address FFF7FA04

Bit 2: IN2 – Reads input value when configures as input

0 = observed at logic level low

1 = observed at logic level high

GPIO_11

Register: FAULTDIR – Fault I/O Direction Register

Address FFF7FA00

Bit 3: DIR3 – Sets I/O direction

0 = configured as input pin (Default)

1 = configured as output pin

Register: FAULTOUT – Fault Out Register

Address FFF7FA08

Bit 3: OUT3 – Sets output value when configured as output

0 = driven low (Default)

1 = driven high

Register: FAULTIN – Fault In Register

Address FFF7FA04

Bit 3: IN3 – Reads input value when configures as input

0 = observed at logic level low

1 = observed at logic level high

GPIO_12 N/A

GPIO_13 N/A

GPIO_14 N/A

GPIO_15 N/A

GPIO_16

Register: UARTIOCTRLTX – UART I/O (TX) Control Register

Address FFF7D834

Bit 1: IO_FUNC – Selects the function for this pin

0 = GPIO mode (Default)

1 = Baud Clock for SCLK, Normal operation for SCI_RX/SCI_TX

Bit 0: IO_DIR – Pin direction when configured as GPIO

0 = Input (Default)

1 = Output

Bit 3: DATA_IN – Data received from pin when configured as input

0 = observed at logic level low

1 = observed at logic level high

Bit 2: DATA_OUT – Data transmitted to pin when configured as output

0 = driven low (Default)

1 = driven high

GPIO_17

Register: UARTIOCTRLRX – UART I/O (RX) Control Register

Address FFF7D834

Bit 1: IO_FUNC – Selects the function for this pin

0 = GPIO mode (Default)

1 = Baud Clock for SCLK, Normal operation for SCI_RX/SCI_TX

Bit 0: IO_DIR – Pin direction when configured as GPIO

0 = Input (Default)

1 = Output

Bit 3: DATA_IN – Data received from pin when configured as input

0 = observed at logic level low

1 = observed at logic level high

Bit 2: DATA_OUT – Data transmitted to pin when configured as output

0 = driven low (Default)

1 = driven high

GPIO_18

Register: T16PWM0CMPCTRL – PWM0 Compare Control Register

Address FFF7FD44

Bits 7-4: OUT_ACTION – Select the function for this pin

0000 = configured as GPIO (Default)

xxxx = PWM0

Bit 9: OUT_ENA – Pin direction when configured as GPIO

0 = configured as an input pin (Default)
 1 = configured as an output pin

Bit 10: OUT – Data to be written into output latch when OUT_DRV = 1
 0 = Output latch is cleared (driven low) (Default)
 1 = Output latch is set (driven high)

Bit 11: IN – Input value when configures as input pin
 0 = Logic level low detected
 1 = Logic level high detected

Bit 8: OUT_DRV – Causes the value of the bit OUT to be written into the output latch. After setting the **OUT** (Bit 10) value, **OUT_DRV** bit needs to be set to one in order for **OUT** (Bit 10) to propagate toward the output and set the output pin state. The bit is a self clearing bit, and always reads as '0'.
 0 = Output latch not affected by the value of **OUT** (Default)
 1 = Value of **OUT** written into the output latch

GPIO_19

Register: T16PWM1CMPCTRL – PWM1 Compare Control Register

Address FFF7FD68

Bits 7-4: OUT_ACTION – Select the function for this pin
 0000 = configured as GPIO (Default)
 xxxx = PWM1

Bit 9: OUT_ENA – Pin direction when configured as GPIO
 0 = configured as an input pin (Default)
 1 = configured as an output pin

Bit 10: OUT – Data to be written into output latch when OUT_DRV = 1
 0 = Output latch is cleared (driven low) (Default)
 1 = Output latch is set (driven high)

Bit 11: IN – Input value when configures as input pin
 0 = Logic level low detected
 1 = Logic level high detected

Bit 8: OUT_DRV – Causes the value of the bit OUT to be written into the output latch. After setting the **OUT** (Bit 10) value, **OUT_DRV** bit needs to be set to one in order for **OUT** (Bit 10) to propagate toward the output and set the output pin state. The bit is a self clearing bit, and always reads as '0'.
 0 = Output latch not affected by the value of **OUT** (Default)
 1 = Value of **OUT** written into the output latch

GPIO_20

Register: T16PWM2CMPCTRL – PWM2 Compare Control Register

Address FFF7FD7C

Bits 7-4: OUT_ACTION – Select the function for this pin
 0000 = configured as GPIO (Default)
 xxxx = PWM2

- Bit 9: OUT_ENA** – Pin direction when configured as GPIO
 0 = configured as an input pin (Default)
 1 = configured as an output pin
- Bit 10: OUT** – Data to be written into output latch when OUT_DRV = 1
 0 = Output latch is cleared (driven low) (Default)
 1 = Output latch is set (driven high)
- Bit 11: IN** – Input value when configures as input pin
 0 = Logic level low detected
 1 = Logic level high detected
- Bit 8: OUT_DRV** – Causes the value of the bit OUT to be written into the output latch. After setting the **OUT** (Bit 10) value, **OUT_DRV** bit needs to be set to one in order for **OUT** (Bit 10) to propagate toward the output and set the output pin state. The bit is a self clearing bit, and always reads as '0'.
 0 = Output latch not affected by the value of **OUT** (Default)
 1 = Value of **OUT** written into the output latch

GPIO_21

Register: T16PWM3CMPCTRL – PWM3 Compare Control Register
Address FFF7FD90

- Bits 7-4: OUT_ACTION** – Select the function for this pin
 0000 = configured as GPIO (Default)
 xxxx = PWM3
- Bit 9: OUT_ENA** – Pin direction when configured as GPIO
 0 = configured as an input pin (Default)
 1 = configured as an output pin
- Bit 10: OUT** – Data to be written into output latch when OUT_DRV = 1
 0 = Output latch is cleared (driven low) (Default)
 1 = Output latch is set (driven high)
- Bit 11: IN** – Input value when configures as input pin
 0 = Logic level low detected
 1 = Logic level high detected
- Bit 8: OUT_DRV** – Causes the value of the bit OUT to be written into the output latch. After setting the **OUT** (Bit 10) value, **OUT_DRV** bit needs to be set to one in order for **OUT** (Bit 10) to propagate toward the output and set the output pin state. The bit is a self clearing bit, and always reads as '0'.
 0 = Output latch not affected by the value of **OUT** (Default)
 1 = Value of **OUT** written into the output latch

GPIO_22

Register: SPIPC6 – SPI Pin Control Register 6
Address FFF7F830

- Bit 1: CLKFUN** – Sets the function for this pin

0 = Configured in GPIO mode (Default)

1 = Configured in SPI mode

Register: SPIPC1 – SPI Pin Control Register 1

Address FFF7F81C

Bit 1: CLK_DIR – Sets I/O direction

0 = configured as an input (Default)

1 = configured as an output

Register: SPIST1 – SPI Pin Status Register 1

Address FFF7F820

Bit 1: CLK_DIN – Input value when configured as input pin

0 = Logic level low observed

1 = Logic level high observed

Register: SPIPC3 – SPI Pin Control Register 3

Address FFF7F824

Bit 1: CLK_DOUT – Output value when configured as output pin

0 = Driven low (Default)

1 = Driven high

GPIO_23

Register: SPIPC6 – SPI Pin Control Register 6

Address FFF7F830

Bit 2: SIMOFUN – Sets the function for this pin

0 = Configured in GPIO mode (Default)

1 = Configured in SPI mode

Register: SPIPC1 – SPI Pin Control Register 1

Address FFF7F81C

Bit 2: SIMO_DIR – Sets I/O direction

0 = configured as an input (Default)

1 = configured as an output

Register: SPIST1 – SPI Pin Status Register 1

Address FFF7F820

Bit 2: SIMO_DIN – Input value when configured as input pin

0 = Logic level low observed

1 = Logic level high observed

Register: SPIPC3 – SPI Pin Control Register 3

Address FFF7F824

Bit 2: SIMO_DOUT – Output value when configured as output pin

0 = Driven low (Default)

1 = Driven high

GPIO_24

Register: SPIPC6 – SPI Pin Control Register 6

Address FFF7F830

Bit 3: SOMIFUN – Sets the function for this pin

0 = Configured in GPIO mode (Default)

1 = Configured in SPI mode

Register: SPIPC1 – SPI Pin Control Register 1

Address FFF7F81C

Bit 3: SOMI_DIR – Sets I/O direction

0 = configured as an input (Default)

1 = configured as an output

Register: SPIST1 – SPI Pin Status Register 1

Address FFF7F820

Bit 3: SOMI_DIN – Input value when configured as input pin

0 = Logic level low observed

1 = Logic level high observed

Register: SPIPC3 – SPI Pin Control Register 3

Address FFF7F824

Bit 3: SOMI_DOUT – Output value when configured as output pin

0 = Driven low (Default)

1 = Driven high

GPIO_25

Register: EXTINTDIR – EXT_INT I/O Direction Register

Address FFF7FA20

Bit 0: DIR0 – Sets I/O direction

0 = configured as an input (Default)

1 = configured as an output

Register: EXTINTIN – EXT_INT IN Register

Address FFF7FA24

Bit 0: IN0 – Input value when configured as input

0 = observed at logic level low

1 = observed at logic level high

Register: EXTINTOUT – EXT_INT OUT Register

Address FFF7FA28

Bit 0: OUT0 –Output value when configures as output

0 = driven low (Default)

1 = driven high

GPIO_26

Register: SPIPC6 – SPI Pin Control Register 6

Address FFF7F830

Bit 4: SCSFUN – Sets the function for this pin

0 = Configured in GPIO mode (Default)

1 = Configured in SPI mode

Register: SPIPC1 – SPI Pin Control Register 1

Address FFF7F81C

Bit 4: SCS_DIR – Sets I/O direction

0 = configured as an input (Default)

1 = configured as an output

Register: SPIST1 – SPI Pin Status Register 1

Address FFF7F820

Bit 4: SCS_DIN – Input value when configured as input pin

0 = Logic level low observed

1 = Logic level high observed

Register: SPIPC3 – SPI Pin Control Register 3

Address FFF7F824

Bit 4: SCS_DOUT – Output value when configured as output pin

0 = Driven low (Default)

1 = Driven high

GPIO_27

Register: EXTINTDIR – EXT_INT I/O Direction Register

Address FFF7FA20

Bit 1: DIR1 – Sets I/O direction

0 = configured as an input (Default)

1 = configured as an output

Register: EXTINTIN – EXT_INT IN Register

Address FFF7FA24

Bit 1: IN1 – Input value when configured as input

0 = observed at logic level low

1 = observed at logic level high

Register: EXTINTOUT – EXT_INT OUT Register

Address FFF7FA28

Bit 1: OUT1 –Output value when configures as output

0 = driven low (Default)

1 = driven high

GPIO_28

Register: SYNCCTRL – Sync Control Register

Address FFF7F024

Bit 0: SYNC_INPUT_DIR – Configure I/O direction

0 = configured as an output pin

1 = configured as an input pin (Default)

Bit 16: SYNC_INPUT_IN – Input value pin when configured as input

0 = Logic level low present

1 = Logic level high present

Bit 1: SYNC_INPUT_OUT – Output value when configured as output

0 = driven low

1 = driven high (Default)

GPIO_29

Register: CLKCNTL – Clock Control Register

Address FFFFFFFD0

Bit 6-5: CLKSr – Set the function of the SYNC_OUTPUT pin.

00 = Configured as a digital input/output pin (Default)

xx = Driven source when used as SYNC_OUTPUT

Register: SYNCCTRL – Sync Control Register

Address FFF7F024

Bit 2: SYNC_OUTPUT_DIR – Configures I/O direction

0 = configured as an output pin (**Note: to use this pin as output, bit 4 “CLKDIR” in register “CLKCNTL” needs to be set to 1**)

1 = configured as an input pin (Default)

Bit 17: SYNC_OUT_IN – Input value when configured as input

0 = Logic level low present

1 = Logic level high present

Register: CLKCNTL – Clock Control Register

Address FFFFFFFD0

Bit 3: CLKDOUT – Output value when configured as output pin

0 = driven to logic low (Default)

1 = driven to logic high

GPIO_30

Register: FAULTDIR – Fault I/O Direction Register

Address FFF7FA00

Bit 4: DIR4 – Sets I/O direction

0 = configured as input pin (Default)

1 = configured as output pin

Register: FAULTOUT – Fault Out Register

Address FFF7FA08

Bit 4: OUT4 – Sets output value when configured as output

0 = driven low (Default)

1 = driven high

Register: FAULTIN – Fault In Register

Address FFF7FA04

Bit 4: IN4 – Reads input value when configures as input

0 = observed at logic level low

1 = observed at logic level high

GPIO_31

Register: FAULTDIR – Fault I/O Direction Register

Address FFF7FA00

Bit 5: DIR5 – Sets I/O direction

0 = configured as input pin (Default)

1 = configured as output pin

Register: FAULTOUT – Fault Out Register

Address FFF7FA08

Bit 5: OUT5 – Sets output value when configured as output

0 = driven low (Default)

1 = driven high

Register: FAULTIN – Fault In Register

Address FFF7FA04

Bit 5: IN5 – Reads input value when configures as input

0 = observed at logic level low
1 = observed at logic level high

GPIO_32

Register: FAULTDIR – Fault I/O Direction Register

Address FFF7FA00

Bit 6: DIR6 – Sets I/O direction

0 = configured as input pin (Default)
1 = configured as output pin

Register: FAULTOUT – Fault Out Register

Address FFF7FA08

Bit 6: OUT6 – Sets output value when configured as output

0 = driven low (Default)
1 = driven high

Register: FAULTIN – Fault In Register

Address FFF7FA04

Bit 6: IN6 – Reads input value when configures as input

0 = observed at logic level low
1 = observed at logic level high

GPIO_33

Register: FAULTDIR – Fault I/O Direction Register

Address FFF7FA00

Bit 7: DIR7 – Sets I/O direction

0 = configured as input pin (Default)
1 = configured as output pin

Register: FAULTOUT – Fault Out Register

Address FFF7FA08

Bit 7: OUT7 – Sets output value when configured as output

0 = driven low (Default)
1 = driven high

Register: FAULTIN – Fault In Register

Address FFF7FA04

Bit 7: IN7 – Reads input value when configures as input

0 = observed at logic level low
1 = observed at logic level high

GPIO_34

Register: T24CAP0CTRL – 24-bit Capture Channel 0 Control Register

Address FFF7FD14

Bits 3-2: EDGE – Set pin function

00 = configured as GPIO (Default)
xx = Capture

Register: T24CAPIO – 24-bit Capture I/O Control and Data Register

Address FFF7FD20

- Bit 0: DIR0** – Sets I/O direction
 - 0 = configured as input (Default)
 - 1 = configured as output
- Bit 2: DIN0** – Input data when configured as input
 - 0 = Logic level low detected
 - 1 = Logic level high detected
- Bit 1: DOUT0** – Output data when configured as output
 - 0 = Logic level driven low (Default)
 - 1 = Logic level driven high

GPIO_35

Register: T24CAP1CTRL – 24-bit Capture Channel 1 Control Register

Address FFF7FD18

- Bits 3-2: EDGE** – Set pin function
 - 00 = configured as GPIO (Default)
 - xx = Capture

Register: T24CAPIO – 24-bit Capture I/O Control and Data Register

Address FFF7FD20

- Bit 03 DIR1** – Sets I/O direction
 - 0 = configured as input (Default)
 - 1 = configured as output
- Bit 5: DIN1** – Input data when configured as input
 - 0 = Logic level low detected
 - 1 = Logic level high detected
- Bit 4: DOUT1** – Output data when configured as output
 - 0 = Logic level driven low (Default)
 - 1 = Logic level driven high

GPIO_36

Register: T24CMP1CTRL – 24-bit Output Compare Channel 1 Control

Address FFF7FD30

- Bit 3-2: OUT_ACTION** – Set pin function
 - 00 = configured as GPIO (Default)
 - xx = Compare
- Bit 5: OUT_ENA** – Sets I/O direction

0 = configured as an input pin (Default)

1 = configured as an output pin

Bit 7: IN – Input Value when configured as input

0 = Logic level low detected

1 = Logic level high detected

Bit 4: OUT_DRV – Causes the value of the bit OUT to be written into the output latch. This bit needs to be set if configured as output pin. The bit is always read as '0'.

0 = Output latch not affected by the value of OUT (Default)

1 = Value of OUT written into the output latch

Bit 6: OUT – data to be written into the output latch when ODRV=1

0 = Output latch is cleared

1 = Output latch is set

GPIO_37 N/A

GPIO_38, GPIO_39, GPIO_40 and GPIO_41 only exist for 64/48/40 pin devices. These devices incorporate an alternate function multiplexer that allow for the 4-wire JTAG port to be used as a SPI port, UART port, sync I/O port, GPIO port or external interrupt port. As some of this function pins are lost when packaging this lower pin count devices. The I/O functional multiplexer control register (IOMUXCTRL) configures the functionalities for these shared pins:

IOMUXCTRL	Bits: 2-0: IO_FUNC_MODE						
Pin# (64/48)	111, 000	001	010	011	100	101	110
39/30	TMS	SPI-CS/GPIO-38	SYNC-OUT	FAULT-2B	INT1	INT1	INT1
38/29	TDI	SPI-DI/GPIO-39	SCI-RX	FAULT-1B	SCI-RX	SYNC-IN	TCAP0
37/28	TDO	SPI-D0/GPIO-40	SCI-TX	SYNC-OUT	SCI-TX	SYNC-OUT	TCOMPARE
36/27	TCK	SPI-CLK/GPIO-41	SYN-IN	SYNC-IN	INT2	INT2	TCAP1

For the 40-pin device, the following table shows six alternative functions selectable by setting the IO_FUNC_MODE bits.

IOMUXCTRL	Bits: 2-0: IO_FUNC_MODE					
Pin# (40)	001	010	011	100	101	110
24	SPI-DI/GPIO-39	SCI-RX	FAULT-1B	SCI-RX	SYNC-IN	TCAP0
23	SPI-D0/GPIO-40	SCI-TX	SYNC-OUT	SCI-TX	SYNC-OUT	TCOMPARE
22	SPI-CLK/GPIO-41	SYN-IN	SYNC-IN	INT2	INT2	TCAP1

NOTE: For code security purpose, customer may need to disable JTAG once the code development is complete.

GPIO_38

Register: IOMUXCTRL – I/O Functional Multiplexer Control Register

Address FFF7F028

Bits 2-0: IO_FUNC_MODE – Provides multiplexing pin options for the JTAG pins in smaller pin package devices

001 = GPIO/SPI mode (Default)

xxx = other function

Register: SPIPC6 – SPI Pin Control Register 6

Address FFF7F830

Bit 4: SCSFUN – Sets the function for this pin

0 = Configured in GPIO mode (Default)

1 = Configured in SPI mode

Register: SPIPC1 – SPI Pin Control Register 1

Address FFF7F81C

Bit 4: SCS_DIR – Sets I/O direction

0 = configured as an input (Default)

1 = configured as an output

Register: SPIST1 – SPI Pin Status Register 1

Address FFF7F820

Bit 4: SCS_DIN – Input value when configured as input pin

0 = Logic level low observed

1 = Logic level high observed

Register: SPIPC3 – SPI Pin Control Register 3

Address FFF7F824

Bit 4: SCS_DOUT – Output value when configured as output pin

0 = Driven low (Default)

1 = Driven high

GPIO_39

Register: IOMUXCTRL – I/O Functional Multiplexer Control Register

Address FFF7F028

Bits 2-0: IO_FUNC_MODE – Provides multiplexing pin options for the JTAG pins in smaller pin package devices

001 = Configured as GPIO/SPI (Default)

xxx = Configured as other function

Register: SPIPC6 – SPI Pin Control Register 6

Address FFF7F830

Bit 2: SIMOFUN – Sets the function for this pin

0 = Configured in GPIO mode (Default)

1 = Configured in SPI mode

Register: SPIPC1 – SPI Pin Control Register 1

Address FFF7F81C

Bit 2: SIMO_DIR – Sets I/O direction

0 = configured as an input (Default)

1 = configured as an output

Register: SPIST1 – SPI Pin Status Register 1

Address FFF7F820

Bit 2: SIMO_DIN – Input value when configured as input pin

0 = Logic level low observed

1 = Logic level high observed

Register: SPIPC3 – SPI Pin Control Register 3

Address FFF7F824

Bit 2: SIMO_DOUT – Output value when configured as output pin

0 = Driven low (Default)

1 = Driven high

GPIO_40

Register: IOMUXCTRL – I/O Functional Multiplexer Control Register

Address FFF7F028

Bits 2-0: IO_FUNC_MODE – Provides multiplexing pin options for the JTAG pins in smaller pin package devices

001 = GPIO/SPI mode (Default)

xxx = other function

Register: SPIPC6 – SPI Pin Control Register 6

Address FFF7F830

Bit 3: SOMIFUN – Sets the function for this pin

0 = Configured in GPIO mode (Default)

1 = Configured in SPI mode

Register: SPIPC1 – SPI Pin Control Register 1

Address FFF7F81C

Bit 3: SOMI_DIR – Sets I/O direction

0 = configured as an input (Default)

1 = configured as an output

Register: SPIST1 – SPI Pin Status Register 1

Address FFF7F820

Bit 3: SOMI_DIN – Input value when configured as input pin

0 = Logic level low observed

1 = Logic level high observed

Register: SPIPC3 – SPI Pin Control Register 3

Address FFF7F824

Bit 3: SOMI_DOUT – Output value when configured as output pin

0 = Driven low (Default)

1 = Driven high

GPIO_41

Register: IOMUXCTRL – I/O Functional Multiplexer Control Register

Address FFF7F028

Bits 2-0: IO_FUNC_MODE – Provides multiplexing pin options for the JTAG pins in smaller pin package devices

001 = GPIO/SPI mode (Default)

xxx = other function

Register: SPIPC6 – SPI Pin Control Register 6

Address FFF7F830

Bit 1: CLKFUN – Sets the function for this pin

0 = Configured in GPIO mode (Default)

1 = Configured in SPI mode

Register: SPIPC1 – SPI Pin Control Register 1

Address FFF7F81C

Bit 1: CLK_DIR – Sets I/O direction

0 = configured as an input (Default)

1 = configured as an output

Register: SPIST1 – SPI Pin Status Register 1

Address FFF7F820

Bit 1: CLK_DIN – Input value when configured as input pin

0 = Logic level low observed

1 = Logic level high observed

Register: SPIPC3 – SPI Pin Control Register 3

Address FFF7F824

Bit 1: CLK_DOUT – Output value when configured as output pin

0 = Driven low (Default)

1 = Driven high